1. (Amended) A semiconductor device comprising:

a semiconductor chip upon which are disposed roughly upon a straight line a plurality of bonding pads containing a first region as a connection region and a second region for making contact with a testing probe, and said first and second regions are lined up in a direction substantially perpendicular to said straight line,

a member provided with a plurality of conductors containing a third region as a connection region electrically connected to each of a plurality of external connection terminals and a securing area for securing said semiconductor chip,

a plurality of conductor wires that electrically connect said first regions of said plurality of bonding pads to said third regions of said plurality of conductors, and

an encapsulating member that encapsulates said semiconductor chip and said plurality of conductor wires.

3. (Amended) The semiconductor device according to claim 1 wherein said plurality of bonding pads are rectangular in shape with their with their short sides lying in a direction along the edges of said semiconductor chip.

4. (Amended) The semiconductor device according to claim 1 wherein said plurality of bonding pads are formed with the width of said first region being wider than the width of said second region in the direction along the edges of said semiconductor chip.

5. (Amended) The semiconductor device according to claim 1 wherein said plurality of bonding pads have notches between said first region and said second region.

6. (Amended) The semiconductor device according to claim 1 wherein said member is an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

7. (Amended) A method of manufacturing semiconductor devices comprising:

disposing roughly upon a straight line a plurality of bonding pads containing a first region as a connection region and a second region for making contact with a testing probe, and said first and second regions are lined up in a direction perpendicular to said straight line, and a member provided with a plurality of conductors containing a third region as a connection region electrically connected to each of a plurality of external connection terminals and a securing area for securing said semiconductor chip are secured, and

disposing a plurality of conductor wires to electrically connect said first regions of said plurality of bonding pads to said third regions of said plurality of conductors.

10. (Amended) The method of manufacturing semiconductor devices according to claim 7 further comprising a step wherein, prior to said securing step, testing of said semiconductor chip is performed by putting test probes into contact with the second regions of said plurality of bonding pads.

Please add new claims 11-19 as follows:

--11. (New) The semiconductor device according to claim 2 wherein said plurality of bonding pads are rectangular in shape with their with their short sides lying in a direction along the edges of said semiconductor chip.

12. (New) The semiconductor device according to claim 2 wherein said plurality of bonding pads are formed with the width of said first region being wider than the width of said second region in the direction along the edges of said semiconductor chip.

13. (New) The semiconductor device according to claim 2 wherein said plurality of bonding pads have notches between said first region and said second region.

14. (New) The semiconductor device according to claim 2 wherein said member is an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the

other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

15. (New) The semiconductor device according to claim 3 wherein said member is an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

16. (New) The semiconductor device according to claim 4 wherein said member is an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

17. (New) The semiconductor device according to claim 5 wherein said member is an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

18. (New) The method of manufacturing semiconductor devices according to claim 8 further comprising a step wherein, prior to said securing step, testing of said semiconductor

chip is performed by putting test probes into contact with the second regions of said plurality of bonding pads.

19. (New) The method of manufacturing semiconductor devices according to claim 9 further comprising a step wherein, prior to said securing step, testing of said semiconductor chip is performed by putting test probes into contact with the second regions of said plurality of bonding pads.--